Appl. No. 10/733,626
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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-13 (canceled)

Claim 14 (currently amended): A method of fabricating stacked gate flash memory cells, comprising the steps of:

providing a substrate;

forming a plurality of parallel long trenches along a first direction in the substrate;

forming a conductive layer and a pair of source regions on ~~the~~ a bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected to the conductive layer;

forming a source isolation layer on each conductive layer;

forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby;

forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer;

forming a pair of inter-gate dielectric layers, respectively overlying the floating gate;

forming a pair of control gates, respectively overlying the inter-gate dielectric layer;

forming ~~a second~~ an insulating layer in each long trench, isolating the control gates;

forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches; and

forming a drain region in the substrate adjacent to each cell trench.

Claim 15 (original): The method as claimed in claim 14, wherein the first direction is perpendicular to the second direction.

Claim 16 (original): The method as claimed in claim 14, wherein the substrate is P-type silicon substrate.

Claim 17 (original): The method as claimed in claim 14, further comprising, before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.

Claim 18 (original): The method as claimed in claim 17, wherein the mask layer is silicon nitride.

Claim 19 (original): The method as claimed in claim 14, wherein the source isolation layer is sequentially formed by LPCVD and HDPCVD.

Claim 20 (original): The method as claimed in claim 14, further comprising, before forming a conductive layer and a pair of source regions on the bottom of each long trench, the step of forming a bottom insulating layer in the bottom of each long trench.

Claim 21 (currently amended): The method as claimed in claim [[14]] 20, wherein forming a conductive layer and a pair of source regions on the bottom of each long trench further comprises the steps of:

forming a source line material layer in each long trench, exposing portions of the bottom insulating layer therein;

removing the exposed bottom insulating layer, partially exposing the sidewalls of each long trench;

forming a first spacer on the sidewalls of each long trench;

etching the source line material layer, exposing portions of the bottom insulating layer adjacent to sidewalls of each long trench;

removing the exposed bottom insulating layer, respectively forming a first sidewall gap on the sidewalls of each long trench;

conformally depositing a polysilicon layer in each long trench, filling the first sidewall gaps;

performing a thermal annealing process, forming a pair of source regions in the substrate adjacent to two sidewalls of each long trench; and

etching the polysilicon layer, leaving portions of the polysilicon layer in the first sidewall gaps adjacent to the source line material layer, forming a conductive layer composed of the

source material layer and the adjacent polysilicon layers in each long trench, wherein the source regions are electrically connected with the conductive layer.

Claim 22 (original): The method as claimed in claim 21, wherein the method for depositing the source line material layer is chemical vapor deposition (CVD).

Claim 23 (original): The method as claimed in claim 21, wherein the method for removing the exposed bottom insulating layer is wet etching.

Claim 24 (original): The method as claimed in claim 14, further comprising, before forming a tunnel oxide layer on two sidewalls of each long trench, the step of performing a threshold voltage implantation on the sidewalls of each long trench.

Claim 25 (original): The method as claimed in claim 14, wherein forming a pair of floating gates on the source isolation layer, and thereby respectively contacting the tunnel oxide layer further comprises the steps of:

conformally depositing a second polysilicon layer in each long trench, contacting the tunnel oxide layers therein;

forming a protective layer in each long trench, exposing portions of the second polysilicon layer;

removing portions of the second polysilicon layer exposed by the protective layer, forming a U-shaped second polysilicon layer therein;

forming a pair of second spacers, respectively disposed on the vertical portions of the U-shaped second polysilicon layer;

removing the protecting layer;

conformally depositing a third polysilcon layer in each long trench; and

etching the third polysilicon layer and the U-shaped second polysilicon layer until the source isolation layer is exposed, leaving a composite polysilicon layer composed of the second polysilicon layer and the third polysilicon layer on the two sides of the long trench as a floating gate, wherein the floating gate is L-shaped or reverse L-shaped (⅃).

Claim 26 (original): The method as claimed in claim 25, wherein the protecting layer is boro-silicate-glass (BSG).

Claim 27 (original): The method as claimed in claim 25, wherein the method for depositing the second spacers is LPCVD.

Claim 28 (original): The method as claimed in claim 25, wherein the second spacer is silicon dioxide.

Claim 29 (original): The method as claimed in claim 14, wherein forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches, further comprises the steps of:

sequentially performing photolithography and etching, defining a plurality of parallel long isolation trenches along a second direction, stopping at the conductive layer therein; and

forming an third insulating layer in each long isolation trench.

Claim 30 (original): The method as claimed in claim 29, wherein the third insulating layer is silicon dioxide.

Claim 31 (original): The method as claimed in claim 29, wherein the method of forming the third insulating layer is low pressure chemical vapor deposition (LPCVD).

Claim 32 (original): The method as claimed in claim 14, wherein forming a drain region in the substrate adjacent to each of the cell trenches further comprises the steps of:

removing the mask layer and the pad oxide layer, exposing a plurality of active areas on the substrate;

performing a drain implantation on the active areas;

performing a thermal annealing process, forming a drain region in the substrate adjacent each cell trench; and

forming a fourth insulating layer on each drain region.

Claim 33 (original): The method as claimed in claim 32, wherein impurities used in the drain region implantation are N-type impurities.

Claim 34 (original): The method as claimed in claim 33, wherein the N-type impurities comprise arsenic (As) ions.

Claim 35 (original): The method as claimed in claim 32, wherein the thermal annealing process is rapid thermal annealing (RTA) process.

Claim 36 (original): The method as claimed in claim 32, wherein the fourth insulating layer is a silicon dioxide layer.

Claim 37 (original): The method as claimed in claim 32, the method for forming the fourth insulating layer is high density plasma chemical vapor deposition (HDP CVD).